REMARKS

Applicant notes with appreciation the finding that claims 2-4, 7-9, 12, 14, 16 and 18 would be allowable if re-drafted in independent form. However, those claims have not been redrafted because it is believed that the base claims are allowable as discussed below.

Claims 1, 5-6, 10-11, 13, 15 and 17 have been rejected under 35 U.S.C. 102 (e) as being anticipated by each of Lee, et al. (U.S. patent 6,075,406) and Nozawa (U S. patent 6,014,177). Those rejections are respectfully traversed, and reconsideration is requested.

As discussed in prior responses, and with reference to Figure 14, the present invention relates to a multiplier circuit that generates an output signal bclk at a rate that is a multiple of an input signal aclk. To that end, a phase comparator 191 directly compares the phase of an edge of an input signal with the phase of an edge of the output signal, that is, through the top feedback loop of Figure 14. Prior art circuits such as illustrated in Figure 16 have not directly compared the two signals but, rather, have inserted a divider 193 between the output and the phase comparator. The divider generated a signal from the output for comparison with the input signal, the generated signal being of the same frequency as the input signal.

Neither of the cited references relates to a multiplier circuit or suggests generating "an output signal at a rate that is a multiple of input frequency of an input signal." Nozawa explicitly states that the frequency of the signal VF follows the frequency of the signal H. See the abstract and the sentence bridging columns 4 and 5. Further, each of Figs. 2, 4A and 4B shows that the frequency of signal VF is the same as that of signal H. Similarly, in Lee et al. at column 1, lines 28-31, the phase and frequency of the output Q always follow the phase and frequency of the input signal IN.

Because each of the cited references is a simple phase locked loop in which the output frequency tracks the input frequency, the output is not a multiple of the input and there would be

no need to include a divider in the feedback circuit. Thus, neither of the references suffers the problem solved by the present invention.

With respect to claims 11, 13, 15 and 17, which recite that the phase comparator relies on combinational logic circuitry, the Examiner has stated that the phase detectors of the cited references would inherently rely on that feature. To the contrary, one would not expect the phase comparators in the disclosed applications to be based on combinational logic circuitry.

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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